Code No. 8329/Inst.

FACULTY OF SCIENCE

B.Sc. VI-Semester (CBCS) Examination, January 2021

Subject : Electronics (Digital System Design Using VHDL)

Paper – VIII- (DSE E – 2)

Time : 2 Hours **Max. Marks: 60**

PART – A

Answer any three questions. **(3x5=15 Marks)**

1 Mention the significance of operators and expressions.
2 Write about the modelling concepts of VHDL.
3 What are procedure parameters? Explain.
4 Explain how Entity declarations are made in modeling.
5 Explain Resolved signals and Ports.
6 What are the uses of clauses in packages?
7 Explain parameterizing structure.
8 Discuss about the case study.

PART – B

Answer any three questions. **(3x15=45 Marks)**

9 Mention about the modeling languages. Discuss Lexical elements and syntax.

10 Discuss about (i) Case statements (ii) Loop statements and Null statements.

11 What are the differences between Behavioural description and structural description? Discuss in detail.

12 What is visibility of Declaration? Explain call statements and overloading with suitable examples.

13 Describe the predefined package standard and write its declaration in detail.

14 Explain IEEE-standard logic Resolved signals.

15 List the different generic constants and discuss its behavioural structures.

16 Explain register-transfer level model of any case study.

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